Abstract

Method for fabricating a contact hole plane in a memory module

In order to fabricate a contact hole plane in a memory module with an arrangement of memory cells each having a selection transistor, on a semiconductor substrate with an arrangement of mutually adjacent gate electrode tracks on the semiconductor surface, an insulator layer is formed on the semiconductor surface and a sacrificial layer is subsequently formed on the insulator layer, then material plugs are produced on the sacrificial layer for the purpose of defining contact openings between the mutually adjacent gate electrode tracks, the sacrificial layer is etched to form material plugs with the underlying sacrificial layer blocks, after the production of the vitreous layer with uncovering of the sacrificial layer blocks above the contact openings between the mutually adjacent gate electrode tracks, an essentially planar surface being formed, then the sacrificial layer material is etched out from the vitreous layer and the uncovered insulator material is removed above the contact openings on the semiconductor surface and, finally, the contact opening regions are filled with a conductive material.

Figure 1H